What is the function of the statement GENERIC, and how can one instantiate a Generic component. i.e How to port map it?

* Generic statement is very useful to make the user control the instantiation of the component with different values for each port map, they are used in different applications, one of these application is our program when we exploit the generate command to generate a clock of periods 0.5s, 1s, 2s, 4s from the 50MHz clock on Spartan 3 board, we put some code here to clarify the way of using generate statement, as you see below the generic statement is placed before the port statement.

entityGenClock is

Generic (time\_period : integer);

Port(clk: in std\_logic;

Clock: out std\_logic);

endGenClock;

In the example below shows how to instantiate Generic component. For example, when we need to instantiate GenClock, we need to put the value of generic as below, if we don't put anything, the default will be used, however in our program we always put a value for the generic, this code pass 25000000 which is considered half second because the one second is 50000000.

time1:GenClock generic map(25000000) port map(clk,led1); ---0.5 second

The code below is for instantiating the component with 2 and 4 seconds:

time3:GenClock generic map(100000000) port map(clk,led3); ---2 second

time4:GenClock generic map(200000000) port map(clk,led4); ---4 second